WHAT IS CLAIMED IS:

1. A fuse latch circuit comprising:

a fuse;

a first inverter in which an input end is connected to one end of the fuse;

a second inverter in which an input end is connected to an output end of the first inverter;

a first transistor in which a first power supply potential is input to a source, a drain is connected to the one end of the fuse, and a pulse signal for initialization is input to a gate;

a second transistor in which the first power supply potential is input to a source, a drain is connected to the one end of the fuse, and a gate is connected to the output end of the first inverter; and

a third transistor in which a second power supply potential is input to a source, a drain is connected to the other end of the fuse, and the pulse signal is input to a gate,

wherein conductance of the first transistor is higher than that of the second transistor.

2. The fuse latch circuit according to claim 1, wherein a circuit threshold value of the first inverter is set to a half value of a total value of the first power supply potential and the second power supply potential.

3. A semiconductor integrated circuit comprising:

a fuse latch circuit group comprised of a plurality of fuse latch circuits; and

an internal circuit which receives output signals of the fuse latch circuit group,

wherein each of said plurality of fuse latch circuits is the fuse latch circuit according to claim 1.

4. A semiconductor integrated circuit comprising:

a plurality of fuse latch circuit groups each comprised of a plurality of fuse latch circuits; and

an internal circuit which receives output signals of said plurality of fuse latch circuit groups,

wherein each of said plurality of fuse latch circuits is the fuse latch circuit according to claim 1, and the pulse signals according to claim 1 are individually fed with different timings into said plurality of fuse latch circuit groups.

5. The semiconductor integrated circuit according to claim 4, wherein the pulse signals according to claim 1 to be individually input to said plurality of fuse latch circuit groups do not overlap timewise with one another.

6. The semiconductor integrated circuit according to claim 5, wherein the timings with which the pulse signals according to claim 1 are individually fed into said plurality of fuse latch circuit groups are controlled by a delay circuit having a delay time

longer than at least a width of the pulse signal.

7. The fuse latch circuit according to claim 1, wherein the third transistor is formed immediately below an end portion of the fuse.

8. The fuse latch circuit according to claim 1, wherein the fuse latch circuit is used for a redundancy circuit of a memory.

9. The fuse latch circuit according to claim 1, wherein the fuse is an aluminum fuse.

10. The fuse latch circuit according to claim 1, wherein the fuse is an electrical fuse.

11. The fuse latch circuit according to claim 1, wherein the first transistor and the second transistor are each a p-channel MOS transistor.

12. The fuse latch circuit according to claim 1, wherein the third transistor is an n-channel MOS transistor.

13. The fuse latch circuit according to claim 1, wherein the second power supply potential is a ground potential.

14. The fuse latch circuit according to claim 1, wherein an output signal of the second inverter is fed into an internal circuit.

15. A memory comprising the fuse latch circuit according to claim 1.

16. A memory comprising the semiconductor integrated circuit according to claim 3.

17. A memory comprising the semiconductor integrated circuit according to claim 4.

18. A memory embedded microcomputer comprising the fuse latch circuit according to claim 1.

19. A memory embedded microcomputer comprising the semiconductor integrated circuit according to claim 3.

20. A memory embedded microcomputer comprising the semiconductor integrated circuit according to claim 4.